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# GENERATION OF 1-BIT FULL ADDER IN CMOS AND TG LOGIC DESIGN FOR LOW POWER APPLICATION

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## ABSTRACT
This paper presents the comparative performance analysis of a 1-bit full adder in two different logic styles CMOS & TG. In this work, the foremost concentration is to lower power dissipation & delay by using the technology scaling approach and developing the circuit to operate at low voltage levels. The circuit interaction is made possible for designing more consistent functional architectures at the minimum power supply of 0.45-1.8v. In the conventional method, two half adders are designed to construct a full adder using an XOR-AND gate to generate a SUM and CARRY( 1-bit) with 28 transistors in static CMOS logic, such a high transistor count to generate 1-bit implies requiring more transistors to generate 4,8,16,32 bit. To minimize the transistor count another logic style called transmission gate (TG) is introduced to design such complex designs in an easier manner. The simulation results of 1-bit full adder CMOS, TG logic are taken from CADENCE Virtuoso in 180, 90 & 45nm technology and the parametric analysis proved better results for TG. This paper presents the comparative performance analysis of a 1-bit full adder in two different logic styles CMOS & TG. In this work, the maximum concentration is to lower power dissipation & delay by using the technology scaling approach and developing the circuit to operate at low voltage levels. The circuit interaction is made possible for designing more consistent functional architectures at the minimum power supply of 0.45-1.8v. In the conventional method, two half adders are intended to construct a full adder using an XOR - AND gate to generate a SUM and CARRY (1-bit) with 28 transistors in static CMOS logic, such a high transistor count to generate 1-bit implies requiring more transistors to generate 4,8,16,32 bit. To minimize the transistor count another logic style called transmission gate (TG) is introduced to design such complex designs in a more accessible manner. The simulation results of 1-bit full adder CMOS, TG logic are taken from CADENCE Virtuoso in 180, 90 & 45nm technology and the parametric analysis proved better results for TG.

**Keywords:** Complementary Metal Oxide Semiconductor (CMOS), Delay, Full Adder (FA), Power Dissipation, Transmission Gate (TG).

## 1. INTRODUCTION
In digital electronic applications like microprocessors, microcontrollers, digital signal processors, etc., the arithmetic unit is a basic building block. Adder is the heart of the arithmetic unit which

performs different operations [1]. In general, the addition will propagate two bit's like a sum and carry, this kind of evaluation is utilized in encoding, decoding, and complementary operations. Each complex adder architecture is built by using Half Adders (HA) and Full Adders (FA). According to Moore's law "For every two years, the transistor count gets double" which means the complexity of the device may vary through timescale from year to year and micro to nanometre as in Fig.1[2]. So, with better technology scaling there is rapid growth in VLSI designs from portable to domestic world in terms of higher speeds, less power consumption, and more reliability. The circuit speed is an important criterion while designing the architecture, and credible achieved by transistor scaling or by limiting parasitic capacitance.

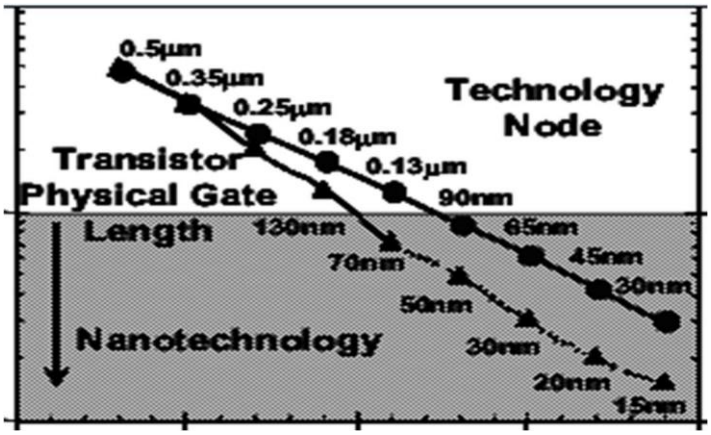



**Fig.1 Transistor size scaling according to Moore's Law.**

Several design approaches are considered to design a FA because of its cascading configuration; these designs are implemented in Complementary Metal Oxide Semiconductor (CMOS) and Transmission Gate (TG) logic. On the other hand, power dissipation leads to increases the circuit complexity in terms of performance degradation. The ultimate goal of researchers is to reduce the power and it always depends upon the switching activity, capacitance nodes, circuit size, etc., in the device level, one of the alternatives is reducing the power supply (Vdd) thus the threshold voltage (Vth) reduces and eventually leads to dropping in power dissipation. However, the foremost impediment is lowering Vdd causes increasing in delay, degrades the circuit drivability based on the logic style chosen. Nevertheless, by selecting the proper aspect ratio (W/L) the power dissipation is trim down rather than lowering Vdd. The circuit delay is another metric, determined by the inversion levels (high to low & low to high states), the transistors count, and the wiring capacitances furthermore predominantly on transistor size in particular channel width & length (W/L) whereas circuit size depends on the transistor count & their sizes and also interconnections [3]. This paper deals with a brief description of the design and implementation of FA in Cadence virtuoso by using different Very Large Scale Integrated (VLSI) technology and its analysis in terms of less power consumption, delay, and power delay product(PDP).

## 2. REALISATION of FA in STATIC CMOS LOGIC

CMOS logic contains P-MOS (P-type MOS) pull up & N-MOS (N-type MOS) pull-down networks. To have a strong one (Vdd) as the output the pull-up network should be designed to ON for low logic values(gnd), henceforth a P-MOS transistor is configured at Pull Up Network(PUN)

[4]. Similarly to have a strong zero (gnd) as the output the pull-down network should be designed to ON for high logic values (Vdd), henceforth a N-MOS transistor is configured at Pull Down Network (PDN) represented in Fig.2.

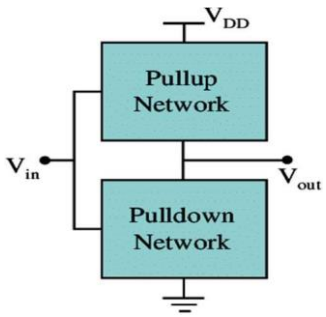
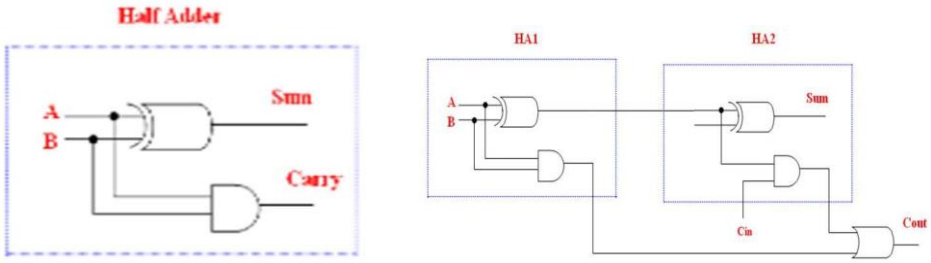



**Fig.2.Generalised structure of CMOS logic style configured with PUN & PDN.**

The conventional FA in static CMOS is realised using HA with XOR-AND gate requires 14 transistors as in Fig.3 (a). XOR gate generates 'Sum' as output & AND gate propagates 'Carry' as Output. Finally for realisation of 1-bit FA it requires 28 transistors with additional 'Carry-in' as input in Fig.3 (b) [5].




**(a). (b).**

**Fig.3 (a) Structure of HA with XOR-AND gate (b) Structure of FA with two HA's**

The FA circuit is designed using CMOS logic with a supply voltage of 1.45-1.8v; through simulation results the delay power dissipation and power delay product (PDP) are calculated. However, the lower supply voltage of 0.8-0.45v degrades the CMOS circuit performance because of leakage current. CMOS logic includes series of transistors to generate output may result in weak output driving capability. Another downside is speed degradation in terms of high input gate capacitance.

## 3. REALISATION of FA in TRANSMISSION GATE (TG) LOGIC

In TG logic P-MOS and N-MOS transistors are connected in parallel and the source & drain terminals are coupled to each other. Here the control input signal access the circuit operation and the bulk terminals are given to respective supply potentials(like P-MOS bulk to Vdd & N-MOS to gnd) to ensure proper signal flow. For example, the HA in Fig.4 is designed by using 8 transistors and all gate terminals act as

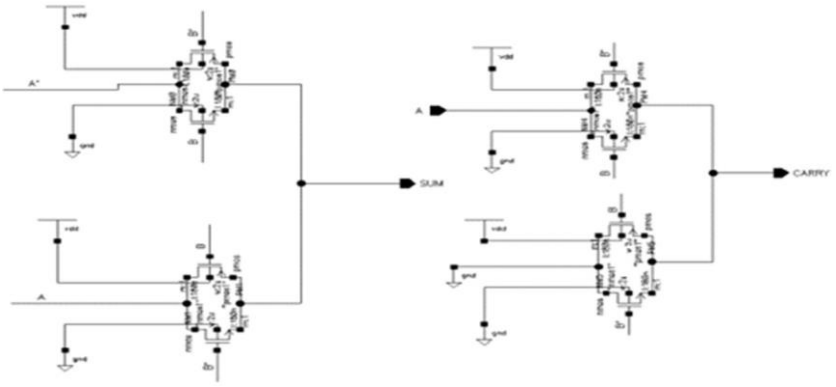
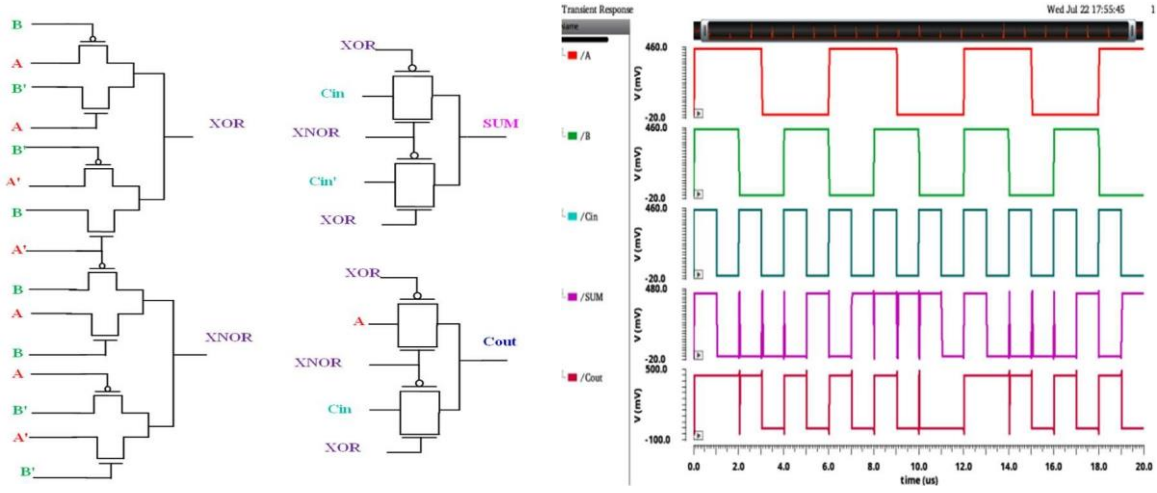



**Fig.4 TG logic HA with 8 transistors.**

controller signals by complimentary connected (B, B'), to generate SUM value:PM0,NM0 drain terminals are pointed with A' & PM1,PM2 drain are pointed with input A and all source terminals are shorted as output. For carry propagation: PM4,NM4 drain are pointed with input A & PM5,NM5 drain terminals are pointed with gnd and all the source terminals are shorted to give CARRY.

## 4. SIMULATION RESULTS

All the simulation results are taken from CADENCE Virtuoso in available technology files like 180nm,90nm & 45nm and TG FA [6] output plot in 45nm with power supply of 0.45v is in Fig.5 illustrate the outputs of SUM & CARRY(Cout) with the delay of 5.0365µs and power dissipation of 52.81pW and all other parameters are tabulated in Table.1. along with power consumption vs. technology in Fig.6




**(a).** **(b).**

**Fig.5 TG logic FA (a).schematic with (b).transient response.**

**Table.1. Power dissipation & delay comparison of FA in CMOS, TG logic.**

| Design | Technology (nm) | Supply voltage(v) | Delay (µs) | Power Dissipation (W) | PDP (j) |
|---|---|---|---|---|---|
| CMOS Logic FA | 180 | 1.8 | 8.958 | 3.177µ | 28.45n |
| | 90 | 0.9 | 8.5 | 226.3n | 0.1923n |
| | 45 | 0.45 | 5.51 | 395.1p | 0.0021p |
| TG Logic FA | 180 | 1.8 | 5.8876 | 1.251µ | 7.365n |
| | 90 | 0.9 | 5.6517 | 98.46n | 0.0556n |
| | 45 | 0.45 | 5.0365 | 52.81p | 0.00026p |

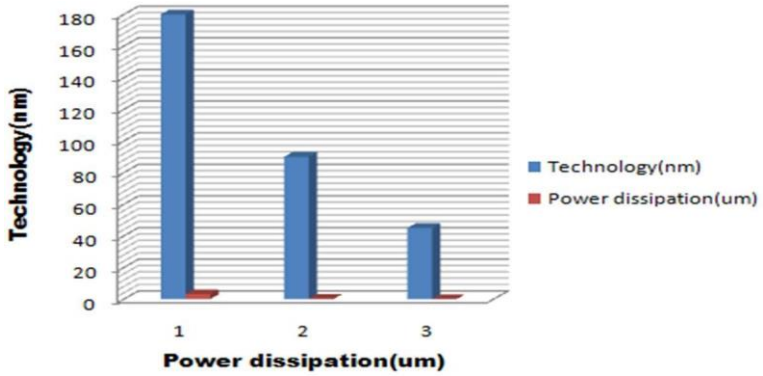



**Fig.6 Power consumption of the TG Full Adder, versus technology**

## 5. CONCLUSION

The simulated result of TG logic FA has revealed better performance than CMOS FA in terms of delay and power consumption with lessen transistor count in 45nm technology at 0.45v and is more sustainable and applicable for low voltage application in the field of VLSI.

## 6. REFERENCES

[1].F. Frustaci, M. Lanuzza, P. Zicari, S. Perri and P. Corsonello, "Designing High-Speed Adders in Power-Constrained Environments," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 2, pp. 172-176, 2009.

[2].Chau, R., Doczy, M., Doyle, B., Datta, S., Dewey, G., Kavalieros, J.,& Radosavljevic, M. "Advanced CMOS transistors in the nanotechnology era for high-performance, low-power logic applications", In Proceedings. IEEE 7th International Conference on Solid-State and Integrated

Circuits Technology, vol. 1, pp. 26-30, 2004.
[3].Wairya, S., Nagaria, R. K., & Tiwari, S, "Performance analysis of high speed hybrid CMOS full adder circuits for low voltage VLSI Design", Hindawi VLSI Design, 2012, doi: 10.1155/2012/173079
[4]. Kirolos, S., Mondal, M., Mohanram, K., & Massoud, Y, "A model-based technique for efficient evaluation of noise robustness", IEEE.50th Midwest Symposium on Circuits andSystems, pp. 714-717, 2007.
[5].Yadav, A. K., Shrivatava, B. P., & Dadoriya, A. K," Low power high speed 1-bit full adder circuit design at 45nm CMOS technology", IEEE International Conference on Recent Innovations in Signal processing and Embedded Systems, pp. 427-432, 2017.
[6]. Mewada, M., Zaveri, M., Gandhi, R., & Thakker, R, "Transmission gate and hybrid CMOS full adder characterization and power-delay product estimation based on mathematical model", Procedia Computer Science, 171, 999-1008, 2020.