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Design of half adder using integrated leakage power reduction techniques

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Abstract

The necessity for the development of compact, portable, and reliable electronic devices of enhanced speed and efficiency has prompted the scaling of CMOS devices to be indispensable. However, the benefit of scaling CMOS devices comes at the cost of increased leakage current in circuits. The variance in power consumption by these circuits incites detrimental impacts on the operational characteristics of the entire device. So, in this work, a novel leakage power reduction technique obtained by combining the Leakage Control Transistor (LECTOR) approach and drain gating approach is proposed. Both these subthreshold leakage minimization approaches are prominently used in Complementary Metal Oxide Semiconductor (CMOS) devices for curtailing the leakage power. The effectiveness of the proposed Integrated Drain Gating Lector (IDGL) technique in mitigating the leakage power is ascertained by designing a half adder circuit. Hence the overall leakage power is of 3.16nW & delay 69.12µs in 180nm technology, and in low scale technology of 90nm the same leakage power decline to 2.19nW & delay is 65.45µs.

Introduction

High performance and increased packing densities characterize modern digital integrated circuits (ICs), which is the product of intensive scaling of devices that occurs with each new phase of advancement in technology. Higher integration improves system reliability while also being incredibly cost-effective due to the reduction in the number of components per system, which successfully lowers packaging and interconnection costs. The operational speed of the circuits has greatly improved as parasitic effects in interconnections have been reduced due to scaling and higher integration. However, on the downside, consumption of power is a major challenge in designing, alongside yield, cost, performance and area, with the rapid rise of portable battery-operated digital devices such as cell phones, multimedia devices, personal digital assistants, laptops, and so on [1], [2], [3], [4], [5].Despite notable advancements in battery technology, the prospect of sweeping transformation in the near future in battery technology is dim due to the limitation in lifetime of the battery.

To scale down the consumption of power under these conditions, it is crucial to develop a circuit with low power design coupled with dynamic power management technique that eliminates the susceptibility to undesirable dissipation of power. To achieve low power consumption, significant attention is laid at each stage of the designing, from the structural level to the physical level. The consistent downscaling of supply voltage is also stimulated due to the demand for reducing the power consumption, since the switching or dynamic power is proportionate to the square of the supply voltage. For avoiding the degradation of performance, scaling of the threshold voltage is also carried out in addition to the scaling of supply voltage. In case of long channel devices, the effect of leakage power is insignificant and does not influence the circuit's operation.

Section snippets

Literature survey

However, band-to-band tunnelling leakage along with oxide leakage is significantly prevalent in technology below 90nm. In digital circuits, the two major classification of power dissipation entails dynamic power dissipation along with static power dissipation as illustrated in Fig. 1. The former takes place during the active mode, when the output node capacitance charges and discharges, whereas the latter takes place during the standby mode due to the existence of leakage current. For…

Lector technique

In order to accomplish leakage power minimization, two additional Leakage Control Transistors (LCTs) are included within the pull-down and pull-up network in case of the LECTOR technique as illustrated in Fig. 2. The infusion of these LCTs is established in a way that the transistor is consistently maintained close to the cut-off voltage. The LCTs assist in substantial reduction of leakage power by enabling the rise in path resistance between the ground and the supply. Since the LCTs are…

Simulation results

Fig. 8 illustrates the simulated outcome of conventional half adder using LECTOR, Drain Gating technique and the Proposed Half Adder with IDGL technique.

The proposed approach's performance against other available strategies in terms of leakage power and delay for 180nm and 90nm technology is given in Table 1 and Table 2 respectively validated from Fig. 8. In case of 180nm technology, the leakage power attained for IDGL based half adder is very low at a value of 3.16nW. Similarly, a minimum…

Conclusion

A highly efficient novel leakage power mitigation approach is developed by integrating LECTOR and Drain gating methods, which are two of the most popular sub threshold leakage minimization techniques. The operational performance of the presented IDGL based leakage reduction technique is evaluated by designing a half adder circuit. The functioning of the half adder circuit designed based on IDGL circuit is compared with conventional half adder circuit and LECTOR based half adder circuit in terms …

CRediT authorship contribution statement

Hima Bindu Katikala: Supervision, Writing – review & editing. **Thatha Pavan Kumar:** Formal analysis, Methodology. **Bhimavarapu Manideep Reddy:** Formal analysis. **Bandireddy V.V.Pavan Kumar:** Writing – review & editing. **G. Ramana Murthy:** Investigation, Validation, Conceptualization. **Saurav Dixit:** Conceptualization, Writing – original draft.…

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Hima Bindu Katikala reports administrative support was provided by Vignan's Foundation for Science Technology and Research.…

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