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RESEARCH ARTICLE

Design and Implementation of High Performance PPSK demodulator in Biomedical Implant

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Abstract

Background/Objective: The important challenge for the realization of hearing aids is small size, low cost, low power consumption, and better performance, etc. Keeping these requirements in view this work concentrates on the VLSI (Very Large Scale Integrated) implementation of the analog circuit that mimics the PPSK (Passive Phase Shift Keying) demodulator with a low pass filter. **Methodology:** This research deals with RF Cochlear implant circuits and their data transmission. A PPSK modulator is used for uplink data transmission in biomedical implants with simultaneous power, data transmission. This study deals with the implementation of a PPSK demodulator with related circuits and a low pass filter which are used in cochlear implants consumes low power and operates at 14MHz frequency. These circuits are designed using FINFET 20nm technology with 0.4v DC supply voltage. **Findings:** The performance of the proposed design over the previous design is operating at low threshold voltage, reduces static leakage currents, and often observed greater than 30 times of improvement in speed performance **Novelty:** As the conventional design with the same supply voltage(0.4v) exhibit high power dissipation and delay and require more amount of time to demodulate the signal. Whereas the proposed FINFET based monostable circuit and PPSK demodulator with a low pass filter has proven better in terms of less delay and power dissipation and can transmit the data with less bit error rate in stipulated time.

Keywords: Cochlear Implant (CI); Fin Field Effect Transistor (FINFET); Electrode Array; Back Telemetry; PPSK Demodulator

1 Introduction

Many wireless medical implants[(1)] are specifically used for prosthesis and diagnosis, functioned to mimic regular body parts. In the field of Pharmacy, designing these implants requires miniaturization of technology & also component scaling. In general, implants are contrived from the skin, bone, tissues & materials-metal/plastic/ceramic,

insertion of nanometer scaled (nm) implant and generation of ionic potential stimulus from the injected electrode array inside the human body through these kinds of the implant is challenging task. The best HYPACUSIS treatment implant is COCHLEAR IMPLANT (CI)[(2)] helps to impetus the auditory nerve directly by stimulating hair cells of the EAR. However, VLSI advanced technologies like CNTFET, FINFET, and TFET makes the scaling of channel width rather than CMOS, leading to certain parametric variations (Power, Delay & Area) accordingly. Designing of implants by incorporating mentioned technologies may enhance the productivity & performance. This research work deals with the exploitation of COCHLEAR implant circuit designing in advanced VLSI technologies. Moore's law[(3)] states for every couple of years, there is a doubling of transistor count on an integrated chip by scaling the technology as in Figure 1. Researchers' progressive efforts from past decades originated a nanometer (nm) technology transistor known as FINFET; shorten the cons of CMOS technology. With FINFET[(4)] narrow channel dual gate structure of Figure 2. Leakage current is lessened & deepens carrier mobility: without increasing doping concentration & require low operating voltage (~0.4v) subsequently condense power dissipation. In evidence to WHO recent proclamation[(5)] 488 million people complain of hearing disabilities for > 40dB echo auditory signals & may extent to >900 million by 2025 via environment conditions, noise pollution, etc., Settling to above strategy research inventors proposing certain medication facilities like artificial implantation (CI) from early 1800 to till date by accommodating electrodes for designing purpose. CI uses 22 active platinum electrodes providing 11 channels as an array, with a length of 17mm, each electrode isolation of <0.1mm & facilitates the biphasic electric stimulus to the auditory nerve[(6,7)] and spiral ganglion nerve in Figure 3.

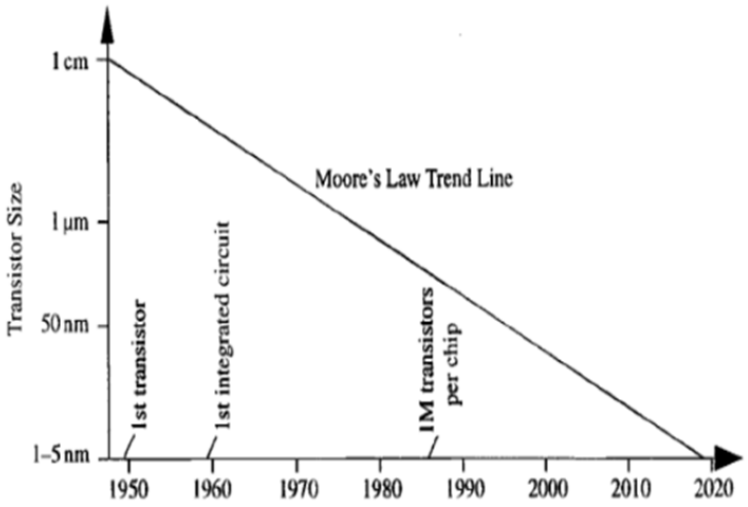

Fig 1. Transistor scaling technology

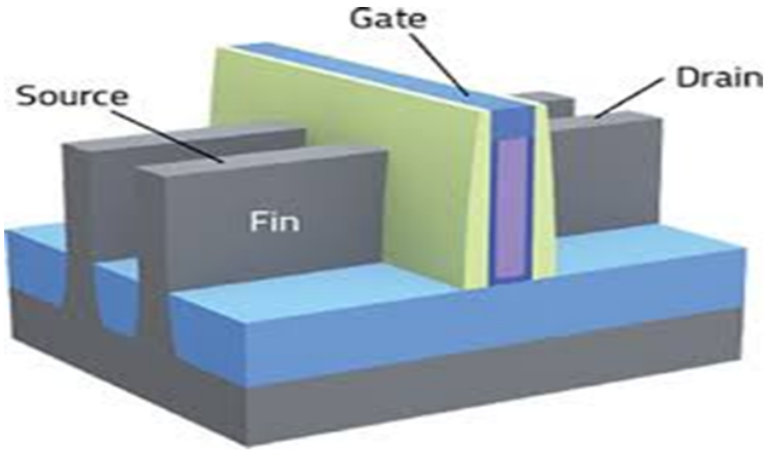

Fig 2. FINFET Planar Structure

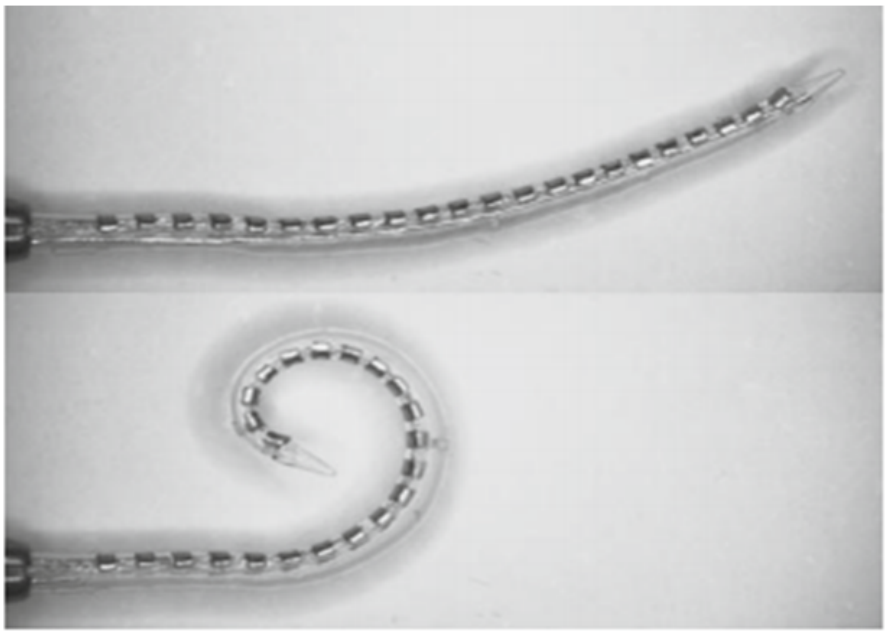

Fig 3. CI Platinum Electrode Array

Conventional CI contains internal parts: Electrode array, transmitter & receiver /Stimulator (9.5 gm) enclosed with external parts: microphone and speech processor. Highly designed CI requires 5-6 hours of surgery for stabilizing hearing sense & placing of Implant inside the ear. Figure 4 describes the signal processing of CI from internal to external parts perfectly.

1. *Speech Processor-receives acoustic signals via microphone*
2. *Transmitter-transmits the encoded audio signals to the internal receiver*
3. *Electrode array-receives transmitted impulses.*
4. *Auditory nerve-The Electrode array electrically stimulates the auditory nerve.*

Table 1 discusses the contribution of an inventor, especially about auditory Neuro-stimulus and their functionalities[8].

Table 1. Invention Route-map of CI

Year	Inventor	Device	Application
1800	Alexandra Volta	Metal rod insertion	Auditory Sensation
1930	Waver- Bray	Auditory nerve connected with electrode	Sound Processing.
1950	Lundeberg	Stimulate Auditory nerve using electricity	Anticipate Processing
1957	Djourna and Eyeries	Stimulate Auditory with current	Perfect Auditory Purpose
1961	House- Doyle	Electrodes insertion for profoundly deaf adults	Clear Auditory Response
1972	Cochlear Corporation	1stsingle channel cochlear implant development	Stimulus functionality
1984	Cochlear Corporation FDA	Wearable Speech Processor ”NUCLEUS”	Speech Coding Strategy
1989	Cochlear corporation	Mini Speech Processor (MSP)	Small size made it suitable for children
2006	Ronald	Advanced Electrolyte Stylet (AOS)	Multi-channel Speech Processor.

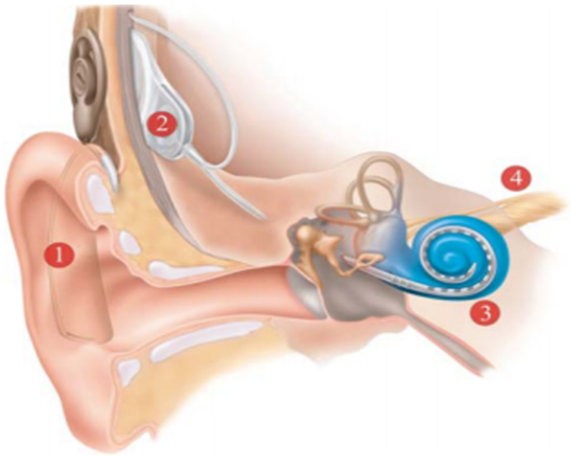

Fig 4. CI Signal Processing

2 FINFET trends in COCHLEAR IMPLANT (CI).

The scope of the electronics in CI is to design the functioning circuits like speech processor, transmitter, etc., by using VLSI technology. The signal processing of the external source to the internal part of the ear is perfectly prototype in Figure 5[(9)]. Modern CI can be successfully progressed by applying a proper synchronized clock implemented in FINFET topology[(10)] that is in Radio Frequency (RF) range. All the medical devices are driven mostly in RF range for ensuring safety interconnect between internal and external parts, to transmit both power and data. The Major sub block is Back telemetry to pretend to monitor the internal unit, electrode unit conditions & neural responses. An ASIC chip with power amplifier[(11)], error frees decoder/demodulator[(12)] and Analog to Digital Converter (ADC) is integrated for internal feedback purpose. However, propagating the signal impulse in move range into the body is crucial task.

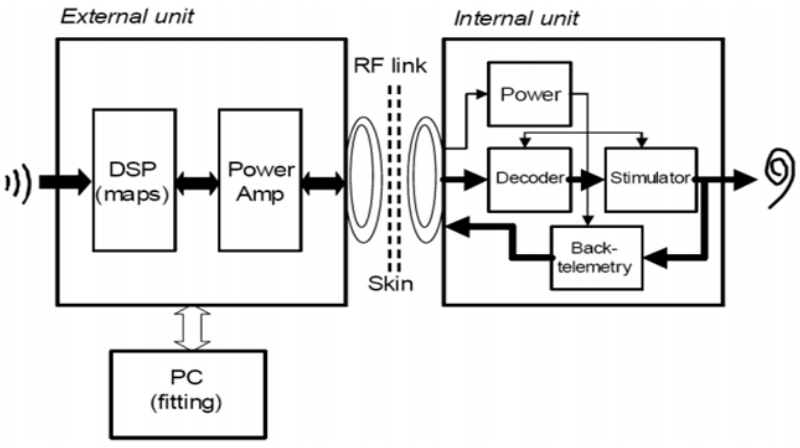

Fig 5. Modern CI Functional Block Diagram.

From the Era of Telephone by Graham Bell in the 18th century, Electrophonic Perception of Stevens with his colleagues in the 19th century, William's Gold Electrode implantable chip in the mid of 19th century proven the audio-signal stimulates in deaf patients & prearranged the trail invention of hearing-aid implantable devices. Various implantable integrated analog circuits have been designed for numerous clinical applications such as cardiac pacemakers, cochlear implants, retinal prostheses, and functional neuromuscular stimulation (FNS) systems. These devices are active implants that require energy sources like solar, infrared & wireless energy transfer for functioning[(13)]. In implanted system, power[(14,15)] is the major concern in the

system design. Due to the lifetime limitation, the battery is not the optimal choice in the implanted device. In recent years, electromagnetic propagation through inductive coupling links is widely used to deliver power and information to these implantable systems.

These approaches can avoid the risk of causing infection and battery life problems. In general, implantable systems must satisfy the following requirements: 1) long-lifetime, 2) high reliability and 3) small size. The implanted device (bio-devices) senses the internal data (body) and converse with the external world by means of power and telemetry [16,17] hence biotelemetry link is used as the bidirectional transmission between bio-device and external tools. The process of data transmission between the bio-device and the tool is in the form of uplink and downlink. Sending of data from the implant to the external world is known as DOWNLINK and its inverse is termed as UPLINK. Bio-device consists of a sensor and a stimulator. The bio-signals are sensed by the sensor and the sensed data is transmitted to the doctors for diagnosis. Multi Stimulator [18] acts as a feedback element that tracks the status of the nerves and the implant. Taking it as a challenge the parts of implantable devices are designed the CMOS technology by considering all technical parametric issues [19]. The main characteristic of an implant is, to modulate the data within the load impedance [20,21] of the inductive link otherwise the increased modulation index decreases the data rate hence the transfer power efficiency decreases [22]. For better modulation, a PPSK demodulator is designed with FINFET technology and compared with existing technology. Based on the considerations, an analog PPSK demodulator communication module circuit is proposed in FINFET technology, because of its low doping concentration with good matching & better performance through proper voltage biasing.

2.1 Conventional PPSK Demodulator

The telemetry circuit implemented in CMOS technology for cochlear implants is shown in Figure 6. It is a surgical device, which senses audio signals from a hearing-impaired person. The device consists of a microphone placed outside the ear and an electrode array in the inner ear and the skin acts as an inductive link between the external and internal parts of the ear. Injecting the device in the exact position of the body takes 6 hours of surgery; however, it should be miniaturized and consume less power.

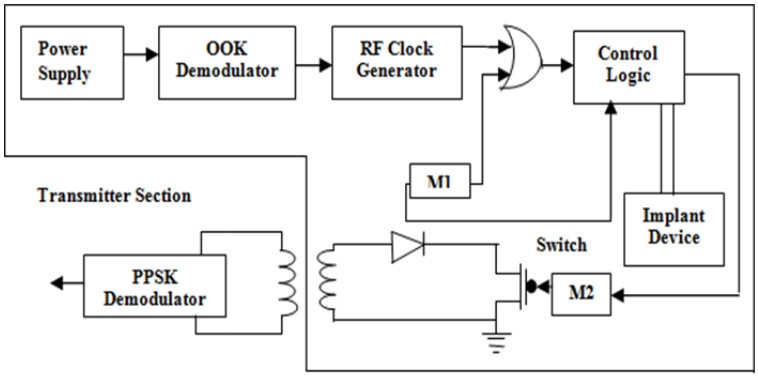

Fig 6. Telemetry Circuit for a Cochlear Implant [16]

2.2 Proposed Telemetry Circuit for a Cochlear Implant

To achieve the desired characteristics of low cost, small size, low power implants, conventional CMOS implants are implemented with 20nm FINFET Technology [23–25]. In this regard, respect RF clock generator, Monostable multi-vibrator, PPSK demodulator are designed and implemented to meet the requirement of the proposed model.

2.2.1 Monostable Multi-vibrator:

In the implant design, a Monostable multi-vibrator is used as the timer to produce the data rate in user-specified time. The proposed circuit is designed with driving large capacitive loads which are implemented using NMOS technology with less delay, a number of stages, and the width value as shown in Figure 7. NMOS inverters are used to amplify the speed and also reduce the transistor count. The two circuits' (M1 and M2) parametric values are the same, but the difference in capacitance C1 (1:5) and the chirality value of width (2). Transistor level implementation of Monostable Circuit is shown in Figure 8

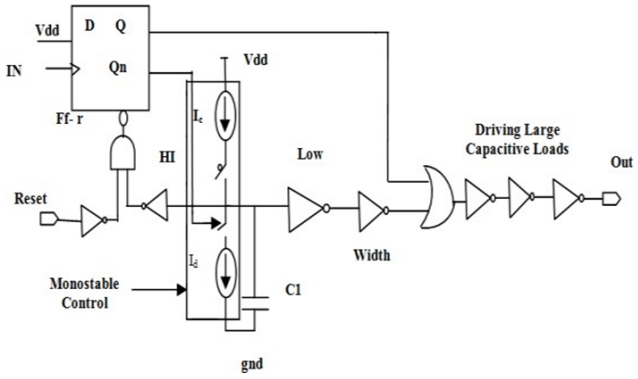

Fig 7. Block Diagram of monostable circuits M1 and M2.

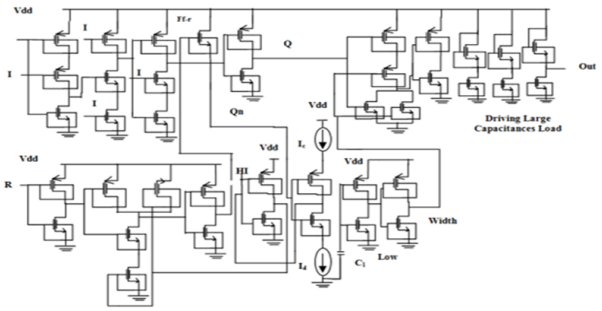

Fig 8. Realization of monostable circuit using FINFET Technology

2.2.2 PPSK Demodulator:

At the external transmitter side, the PPSK demodulator is considered. Comparing with the other modulation techniques the efficient way for authorizing data is done by using PSK[26]. In the proposed circuit an active low pass filter in place of the comparator is used to achieve good modulation by dragging sufficient power to amplify the output signal with low noise as shown in Figure 9. The first-order low pass filter is driven by resistor R and Capacitor C it only allows low-frequency signals but attenuates the signals beyond the cutoff range. As the sine wave response is applied and it generates the triangular wave output by varying C either by charging or by discharging, hence it acts as an Integrator. Chosen R, C (τ) values are greater than the input time period.

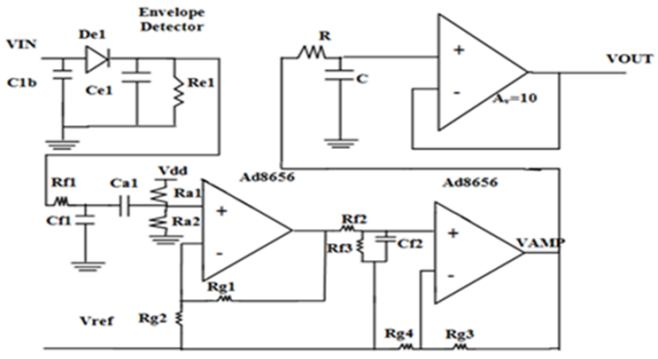

Fig 9. Architecture of Active Low Pass Filter PPSK Demodulator.

2.2.3 Calculation for Bit Error Rate (BER) of Monostable Circuit:

For example, of the generated output of the Monostable circuit, the change of a number of bits of transmitted input (IN) 12Kbits to receive output bits with an error of 4 bits (VOUT) is defined as BER. So error bits are four divided by 12K transmitted bits. The error rate is 0.0000333.

3 Simulation Results

3.1 Monostable Circuits

The simulated waveform for M1 and M2 circuits is generated by FINFET 20 nm technology using the cadence tool by applying 0.4v. As per the transient analysis, the settling time is considered as 7ns for data transmission consequently, the frequency range is of 14MHz Table 1. The delay, dynamic power dissipation is calculated as shown in Table 2. From the waveform, the capacitor C1 alters when FF-reset changes from 1 to 0 and Width from 0 to1, with reference to the time axis, the generated output is amplified in accordance with the width and C1, and it is evident for the less propagation delay in signal transmission from the obtained results of Figure 10.

Table 2. Features Summary

Technology	FINFET 20nm
Design Tool	CADENCE
Supply Voltage	0.4v
Telemetry Specifications	UPLINK
Monostable frequency range	14MHz
Programmable Monostable Circuits (M1,M2)	Implemented using Driving Large Capacitive Loads
Monostable Bit Error Rate	0.0000333
Uplink Modulation	PPSK using Low pass filter

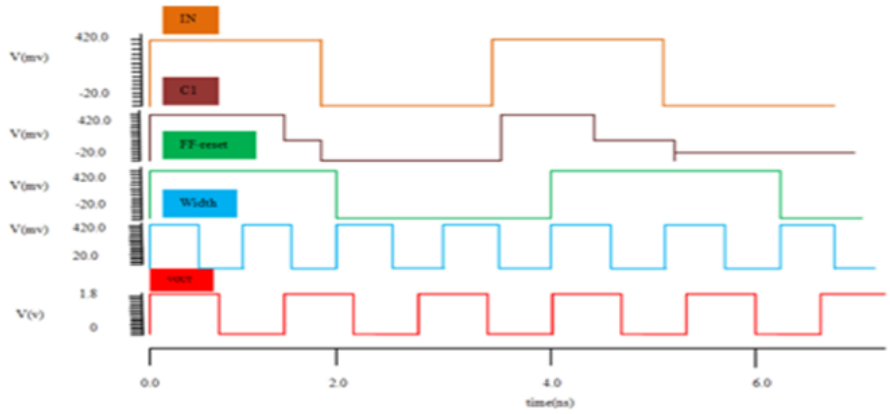

Fig 10. Transisent response of monostable (m1, m2) circuits

3.2 PPSK Demodulator:

PPSK demodulator is implemented with 0.4v supply voltage in 20 nm FINFET technology here VIN, VAMP, a low pass filter capacitor C are the inputs, and VOUT is the output. The simulation results are shown below. It is observed in Figure 11. VOUT is dependent on the C which remains constant until capacitor charges and discharges and changes its phase of the next cycle (VIN) and specifications are tabulated in Table. II, III. Finally, the findings in the paper [27] are more suitable for the design of a demodulator majorly considerable for biomedical implant application.

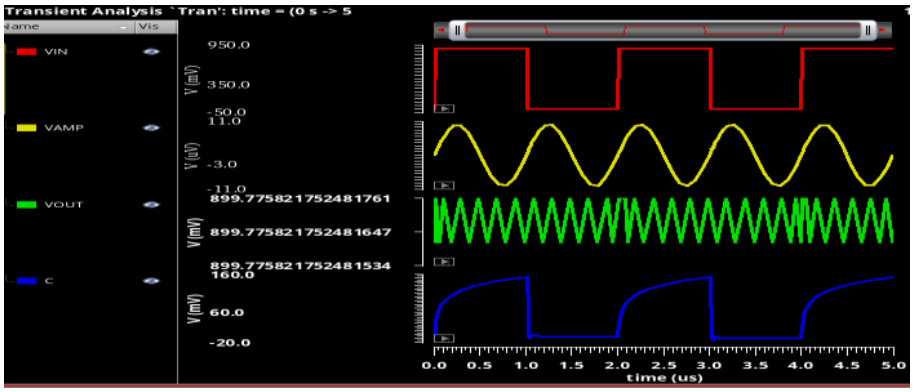

Fig 11. Transient Analysis of PPSK Demodulator

Table 3. Parameters Comparison

Design	Delay(ns)	Dynamic Power Dissipation(μW)	Power Delay Product PDP (j)	Current Consumption(A)
CMOS Monostable Circuit	116.3	8.29	0.096p	1.26m
FINFET Monostable Circuit	3.3825	5.38	0.018p	0.81μ

4 Conclusion

In this paper, Monostable and RF Clock Generator are implemented for cochlear implant application in 20nm FINFET Technology. The existing comparator is replaced by an Active Low pass filter to achieve high accuracy. The conventional monostable circuit is reinstated with driving large capacitive loads to reduce complexity. It is observed that the performance of the proposed design is improved to a large extent, with reduced delay to 34.38% and power dissipation to 1.54% with respect to the conventional methods in CMOS. Hence, by using this advanced FINFET technology the performance is increased by 30%.

Author Contributions

Yatavakilla Amarendra Nath prepared the research methodology and idea for comparative study. All the simulations design, study, and manuscript preparation are done by Hima Bindu Katikala who was assisted by both G.Ramana Murthy and Yatavakilla Amarendra Nath. Result analysis and manuscript proofreading are verified by Professor G.Ramana Murthy.

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